ABSTRACT OF THE DISCLOSURE

A plurality of unit areas having one to a plurality of MOSFETs for implementing specific logic circuits are placed in a first direction. A first interconnection extending in the first direction is formed over each unit area. A second interconnection extending in the first direction is formed along the plurality of unit areas and outside the unit areas. Wiring dedicated areas provided with a third interconnection extending in a second direction intersecting the first direction are respectively provided between the adjacent unit areas. A logic circuit formed in each unit area has both a first connection form connected to the first interconnection and a second connection form connected to the third interconnection, via the second interconnection, according to combinations with the wiring dedicated areas adjacent thereto, as needed.